

**Amendments to the Specification:**

Please replace the paragraph that begins at page 7, line 12 with the following amended paragraph:

The substrate 100 has a p-doping of about  $3 \times 10^{15} \text{ 1/cm}^3$ . On a surface 102 of the substrate 100 a gate structure 104 is formed including a gate polysilicon 106 and a gate oxide 108 arranged between the gate polysilicon 106 and the substrate 100. Within the substrate 100 further an  $n^+$ -source area 110 and an  $n^+$ -drain area 112 is formed. The regions 112a, 112b, 112c indicate drain area regions with different doping concentrations. Below the gate oxide 108 a laterally diffused channel area 114 is formed comprising a p-doping in the area of about  $2 \times 10^{17} \text{ 1/cm}^3$ . The source area 110 and the drain area respectively comprise n-dopings of about  $2 \times 10^{20} \text{ 1/cm}^3$ .

Please replace the paragraph that begins at page 9, line 27 with the following amended paragraph:

~~Fig. 2~~ Curve 2 shows the course of the input characteristic line after the additional p-region 118 was implanted into the LDD area 116. As it may be seen, hereby the characteristic line is lowered, as due to the p-region 118 the resistance in the LDD area 116 is increased and so the drain current compared to the LDD area correspondingly decreases without an additional p-region 118 (curve 1).